Claims:

1. A method for manufacturing a power semiconductor device comprising the steps of:
forming a gate trench mask with open and closed regions on the surface of a semiconductor substrate;
removing semiconductor material from areas exposed by the open regions of the trench mask to form a plurality of gate trenches;
forming a gate oxide layer on the sidewalls of the trenches;
depositing a layer of conductive material on the surface of the substrate and in the trenches;
removing the conductive material from the surface of the semiconductor substrate and leaving enough conductive material in the trenches to substantially fill the trenches;
implanting the substrate with a source dopant to form heavily doped source regions in the surface of the semiconductor substrate;
depositing a metal layer over the substrate;
reacting the metal layer with the substrate to form a thin layer of highly conductive material on the source regions;
depositing a layer of insulating on the substrate;
forming a contact mask of open and closed regions on the insulating layer and removing insulating material from open regions to expose portions of the surface having the highly conductive material on the source regions;
depositing and patterning a conductive layer over the surface of the substrate to form electrical contacts to the highly conductive material on the source regions.

2. The process of claim 1 wherein the substrate comprises silicon and the metal deposited on the source regions is reacted with the substrate to form a silicide.

3. The process of claim 1 wherein the metal on the source regions is platinum or titanium.

4. The process of claim 1 wherein the insulating material is on or more of the materials selected from the group consisting of BPSG, PSG, silicon dioxide and silicon nitride.

5. A power semiconductor device with trench gates comprising:
a semiconductor substrate;
a source layer at one surface of the substrate and comprising a high concentration of a dopant of one polarity;
a well layer beneath the source layer doped with a dopant of opposite polarity;
a plurality of trenches penetrating the source layer, said trenches substantially filled with conductive material;
a highly conductive layer on the surface of the source layer comprising a material reacted from a metal the semiconductor substrate;
an insulating layer on the highly conductive layer;
vias formed in the insulating layer and extending to the highly conductive layer on the source layer;
conductive material filling the vias for contacting the highly conductive layer.

6. The power semiconductor device of claim 5 wherein the substrate comprises silicon and the highly conductive layer on the surface of the source layer is a silicide.

7.. The power semiconductor of claim 6 wherein the silicide is platinum silicide or titanium silicide.

8. The power semiconductor of claim 5 wherein the insulating material is on or more of the materials selected from the group consisting of BPSG, PSG, silicon dioxide and silicon nitride.

9. The power semiconductor device of claim 5 further comprising a drain layer on the other surface one surface of the substrate doped with a high concentration of a dopant of one polarity to form a power MOSFET.

10. The power semiconductor device of claim 5 further comprising a third layer beneath the well layer and comprising dopants of the one polarity and a cathode layer on the opposite surface of the substrate and highly doped with dopants of an opposite polarity to form a power thyristor.